ARMY RESEARCH LABORATORY

Design Report for Low Power Acoustic Detector

by Brian T. Mays

ARL-TR-6552 **August 2013**

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14. ABSTRACT
The Intelligence, Surveillance, and Reconnaissance (ISR) Technology Integration Branch of the U.S. Army Research Laboratory (ARL) in support of persistent surveillance missions has developed a low-power acoustic detector (LPAD). The motivation for this work focused on the development of a system to detect targets with internal combustion engines, which include vehicles, boats, aircraft, and generators, while having an operational life greater than one year on a single AA lithium battery. The LPAD will serve as a wake-up trigger for larger and more power consuming sensors and algorithms such as imagers, array signal processors etc. This report details the hardware design, target detection algorithm design in both MATLAB and VHDL, and typical performance results.

15. SUBJECT TERMS
Acoustic low power, FPGA, Harmonic energy detector, UGS, wake-up trigger

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1. Introduction

1.1 Background

A primary research area of the Intelligence, Surveillance, and Reconnaissance (ISR) Technology Integration Branch of the U.S. Army Research Laboratory (ARL) is persistent surveillance. The class of persistent surveillance requires that sensors operate in a continuous mode over the entire mission life. Typical sensor requirements for mission life are 6 months to several years. Unattended ground sensors (UGS) are a common class of sensors routinely employed by ARL to meet ISR mission needs. While many commercial-off-the-shelf (COTS) and legacy Government-off-the-shelf (GOTS) UGS systems are available, most are not able to meet extended mission life requirements. The key in meeting extended mission life requirements is designing a low-power sensor that can detect the target class of interest in conjunction with an energy-efficient algorithm to exploit the target signature structure. False alarms must be minimized due to the large power penalty in alerting the full UGS.

The motivation for this work focused on the development of a system to detect targets with internal combustion engines, which include vehicles, boats, aircraft, and generators. This report details the design of the low-power acoustic detector (LPAD). The LPAD will serve as a wake-up trigger for larger and more power consuming sensors and algorithms such as imagers, array signal processors etc. The first generation LPAD developed is shown to scale in figure 1. The mechanical form factor was driven by making the unit as small as practical while controlling manufacturing costs. The initial goals of this project were to develop a system that could operate continuously for 1 year and provide simple open collector switch closure to arm more sophisticated electronics.

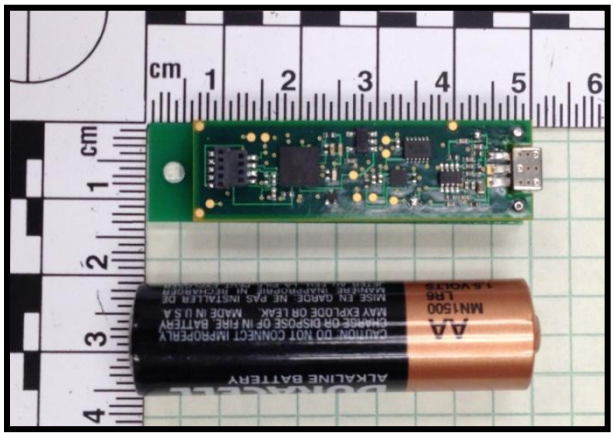

Figure 1. Complete LPAD.

1.2 Theory of Operation

Internal combustion engines produce an audio spectrum that is rich in harmonic structure. The harmonic structure is directly related the periodic cylinder firings of the engine (*1*). Since the energy released from the fuel in the cylinders produces pulsed acoustic waves that propagate from the exhaust and hence are airborne, this energy and channel are common to the targets in our class of interest. The acoustic energy allows detection with simple low-power microphones readily available as COTS items. Figure 2 shows the acoustic spectrogram plot of power boat departing from near the sensor location. At approximately 20 s, the boat throttles up to full RPM and begins to accelerate away from the sensor. The strong harmonic structure of the engine signature is evident in the received sensor data.

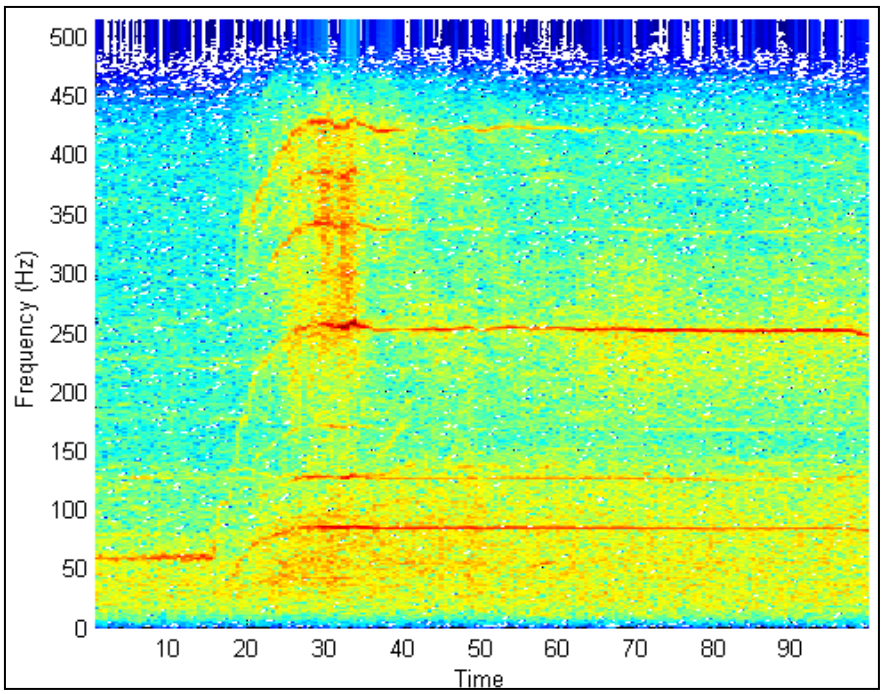

Figure 2. Spectrogram of departing boat.

The strong tonals differentiate the target from the common background acoustic noise sources such as wind, which has a 1/f structure and potentially high amplitudes, and transients, which have a short duration. A key design point in creating an energy-efficient algorithm is processing the minimum information required to detect the targets of interest. In the case of internal combustion engines, significant information can be exploited solely in the frequency domain, allowing amplitude to be ignored. This enables the system to determine a minimum detectable acoustic signal and then simply quantize to 1-bit values using a comparator. This 1-bit processing scheme is central to the energy efficiency of the hardware and the algorithms used to process the data.

2. System Design

2.1 System Architecture

The LPAD has four primary components:

- Microphone
- Analog signal conditioning
- 1-bit digitizer
- Field-programmable gate array (FPGA)-based signal processing

Figure 3 shows a block diagram of the LPAD.

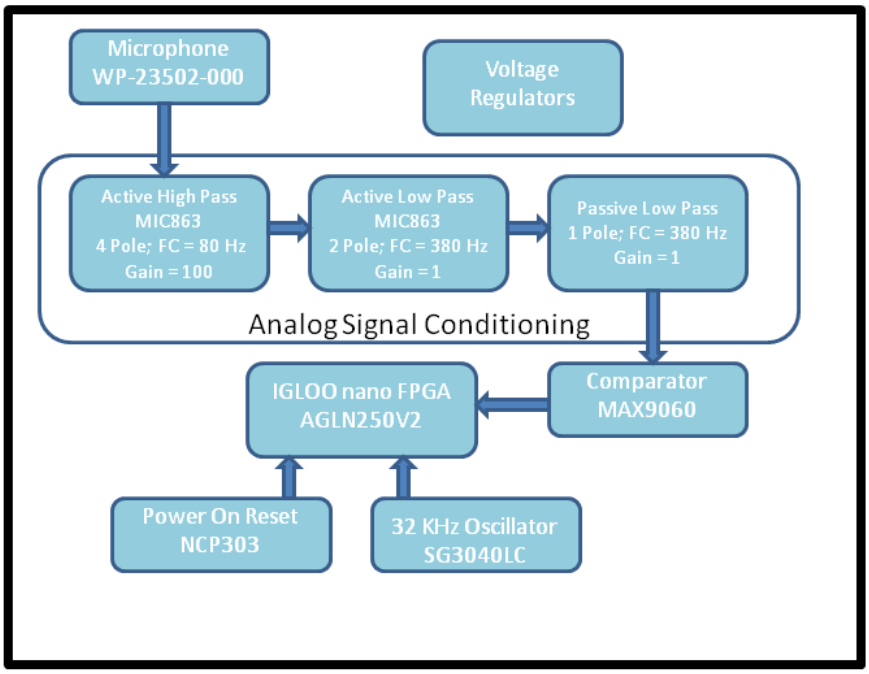

Figure 3. LPAD block diagram.

The LPAD schematics are provided in appendix A.

2.2 Electrical Design

The microphone selected is manufactured by the Knowles Corporation and is from their waterproof line. The specific model used is WP-23502-000 with the following key features:

- Size: 5.56 mm L x 3.99 mm W x 2.26 mm H

- Sensitivity: –52 dBV ±3 dB at a 74-dB sound pressure level (SPL)
- Frequency Range: 100 Hz ~ 4 kHz
- Max Operating Current: 50 µA

The analog front end is designed to pass spectral content from 80 to 380 Hz using a combination of active and passive filters. A primary consideration for the design was to minimize the power consumption and overall size of the filter. The concern for power consumption limited the number of stages used in the active portion of the filter and the effective gain bandwidth of the op amps selected. The size constraint limited the passive filter portion of the circuit. In general, this filter would fall into a general anti-aliasing design, which was only concerned with rejection above Nyquist frequency. In this design, having strong rejection near DC (0–25 Hz) was a concern due to acoustic wind energy present as a 1/f spectrum. To minimize the effects of wind, more poles of the filter were allocated to the high pass portion of the filter. While this tradeoff increases the amount of aliasing, in this specific case of harmonic detection, aliased energy will appear in the spectrum as additional tonals. Since the time domain is not directly processed, this distortion is not critical to the detection process. The first section of the filter is an active 4-pole active high pass filter with a cut-off frequency of 80 Hz and a gain of 100. This section is followed by a large DC blocking capacitor to remove any DC offset introduced by the high gain of the first stage, ensuring the signal isn't shifted away from the comparators sampling point. The next stage is a 2-pole low pass active filter with a cut-off frequency of 380 Hz and unity gain. This stage is followed by a single-pole passive filter with the cut-off also set to 380 Hz. These two stages form the anti-aliasing portion of the filter while ensuring the single maintains proper bias point as presented to the comparator. The operation amplifiers selected were microchip with a quiescent power consumption of 4.2 µA per channel. These low-power op-amps have very low gain bandwidth product (GBW) of 450 KHz, which was also a limiting factor in the filter design and performance.

The comparator selected was MAX9060 from Maxim Integrated. Its low maximum quiescent current of 1.1 µA and ±12 mv of hysteresis make it an excellent 1-bit analog to digital (A/D) converter. The hysteresis allows a minimum acoustic SPL to be set as a design parameter. In this design, a minimum detectable level of 50 dB SPL was selected, equating to a required gain of 40 dB for the microphone selected. This 1-bit signal is simply sampled by the FPGA to complete the digitization process.

The "IGLOO nano" family of low power FPGAs from Actel was selected for superior power consumption performance compared to other vendor offerings. The AGLN250 in the CS81 package (4 mm x 4 mm) was used in the implementation. The IGLOO operates with a core voltage of 1.2 V, which is also attractive for low-power applications.

2.3 Algorithm Design

The initial algorithm design was inspired by the work done by Goldberg et al. (*2*), in which the authors developed a periodic measure (PM) of a random signal. This PM statistically measures the "spikiness" of a signals autocorrelation function (ACF). This statistic is useful for detecting the general class of combustion engines due to the strong periodic nature of the signal. Periodic signals will have dominant peaks in their ACF at lags related to their engine firing rates. Wind noise and other broadband sources will not have multiple strong peaks in the ACF, making this statistic suitable as a detection criterion. A summary of the equations of the PM from (*2*) is repeated (equations 1–4) and is also referred to as the harmonic energy detector (HED):

$$Rxx[n] = \left(\frac{1}{K}\right)\sum_{k=0}^{k=K-1} x[k]x[k+n] \tag{1}$$

$$PM = \sum_{n=Nmin}^{Nmax}(Rxx[n+1] - Rxx[n])^2 \tag{2}$$

$$\tilde{R}xx[n] = \sum_{k=0}^{K-1} [XNOR(x[k], x[k+n])] \tag{3}$$

$$\widetilde{PM} = \sum_{n=Nmin}^{Nmax}\left|\tilde{R}xx[n+1] - \tilde{R}xx[n]\right| \tag{4}$$

Critical to the energy efficiency of the estimate is the fact that the data are 1-bit data, allowing all multiplications in the ACF to be performed by simple XNOR logic operations, as shown in equation 3. Also the sum of the squares calculation is replaced by the sum of the absolute values indicated in equation 4.

The author in this report extends this detection scheme by adding an additional statistic, which measures the change in the ACF over a specified time period. This detector is referred to as the delta correlation detector (DCD). The physical motivation for this measurement is that targets of interest will exhibit a Doppler shift as they pass closest point of approach (CPA) moving the peak location in the ACF spectrum. The additional statistic also covers three common scenarios in which the HED had limited performance: detection at low signal to noise, detector capture, and detection of non-harmonic targets. The DCD accomplishes this by measuring a change in the ACF over a fixed window of time, for example, 30 s. Capture or continuous retrigger is avoided if a nearby harmonic source loiters for long periods or urban noise is present producing high amounts of acoustic energy but spectrally stationary content. The change in the ACF doesn't require harmonic structure, it simply measures that some new structure is present. In general, this can be used as an earlier detector because a lower signal to noise is required than with the PM technique. The additional computational load is minimal as both algorithms require the base ACF calculation and this algorithm merely maintains history of the ACF to build the statistic. The detectors can be used independently or jointly. Initial implementations focused on using these jointly to increase the probability of detection of the target near CPA while avoiding capture from persistent sources in the background spectrum. Equation 5 for the DCD is shown below.

$$DCD = \sum_{LAg=1}^{Lag=MaxLag}\left[\left(\sum_{Win=1}^{MaxWin}\left|\tilde{R}xx[Lag][Win] - \tilde{R}xx[Lag][0]\right|\right)/MaxWin\right] \quad (5)$$

2.4 Algorithm Implementation

The algorithms were first prototyped in MATLAB and are include in appendix B for reference. The first effect modeled was to compare performance between the full fidelity PM calculation and the 1-bit PM calculation. The 1-bit model also includes hysteresis to account for the nonlinearity of the 1-bit A/D conversion process. The MATLAB algorithm was used in developing operating statistics and thresholds by processing bulk data sets collected against various targets. Examples of these results are discussed in the next section.

The next phase of development focused on the very high speed integrated circuit (VHSIC) hardware description language (VHDL) implementation of both the HED and DCD detectors. Figures 4 and 5 show the block diagrams for the algorithm implementations. Note that each algorithm contains three core processes and that process 1 and 2 are identical in both detector schemes. Process 1 samples the 1-bit data from the comparator output and maintains the history length of data required to perform the ACF over the desired delay range. This process is operating at a 1-KHz rate. Process 2, which is also running at a 1-KHz rate, calculates the ACF over 1-s block periods of data. The ACF values are accumulated for the desired delay terms and are presented to process 3 on 1-s boundaries of data. For the HED detector, process 3 calculates the final statistic by taking the absolute value of the pair wise difference terms in the ACF spectrum. To minimize hardware requirements, only one calculation per clock cycle is performed because this process has 1 s to complete prior to next available ACF measureable data. This process is also operating at 1 KHz.

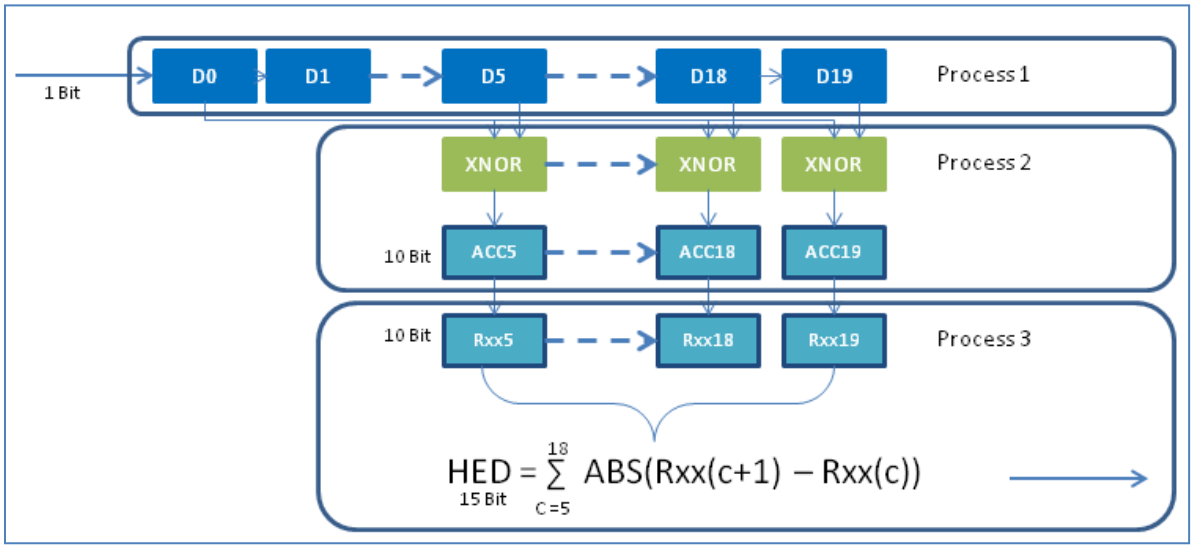

Figure 4. HED VHDL block diagram.

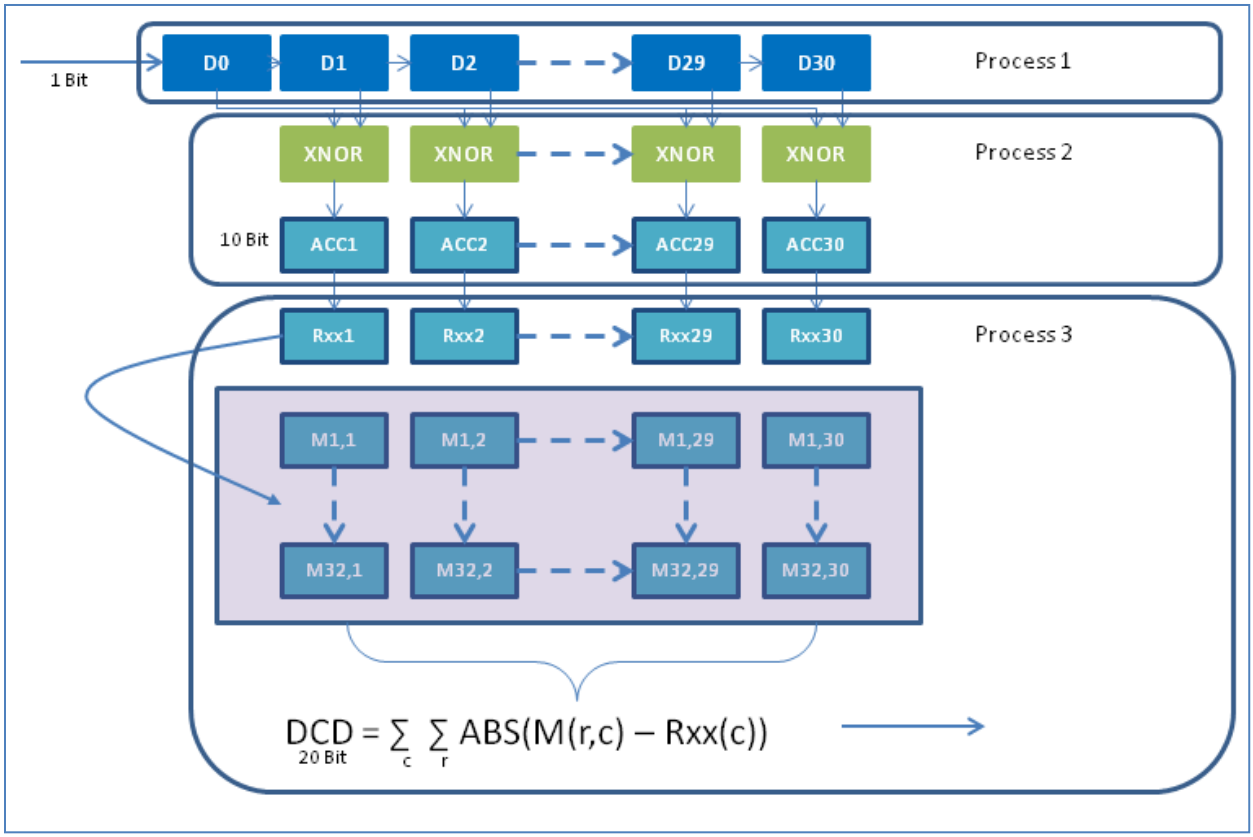

Figure 5. DCD VHDL block diagram.

The DCD detector shown in figure 5 again uses process 1 and 2, as described above, to compute the ACF over 1-s blocks of data. In process 3 of the DCD, RAM block assets of the FPGA are used to maintain a history of the ACF functions over a 32-s window. The ACF history buffer is maintained as a circular buffer by process 3, in which the most recent ACF results replaces the oldest ACF results. Once the buffer is updated, process 3 begins the calculation of the DCD formula with one calculation per clock cycle to minimize hardware requirements during synthesis. With this configuration of ACF time history and ACF length, the number of calculations approaches 1000, so operating on the 1-KHz clock is marginal. For this reason, the initial implementation runs process 3 at 32 KHz to ensure ample time to complete prior to next ACF result set from process 2 being produced. Note that in both detectors all the registers are optimize to use the minimum number of bits for hardware efficiency and are specified in the block diagrams.

The complete top-level schematic of the FPGA implementation is shown in appendix C. This includes HED and DCD detectors, control logic for external hardware wake-up, and raw detector data output via universal asynchronous receiver transmitter (UART) for engineering development. Table 1 shows the post-synthesis FPGA use of the IGLOO AGLN250.

Table 1. FPGA resource use.

FPGA Resource	Used	Total	Percent Usage
CORE	4057	6144	66%
IO (W/ clocks)	35	60	58%
GLOBAL	6	18	33%
RAM/FIFO	5	8	62%

3. Testing Results

3.1 MATLAB-Based Data Processing of Field Test Data to Select Thresholds

Data sets were collected over a 24-h period from a rural harbor entrance. This harbor is used by very few watercrafts per day and is several miles from a major highway. This data set provides representative background data and was used to determine operating thresholds for the detectors. The data sets were not segmented to exclude periods were targets were present, so the processed data does contains some target events and doesn't represent a true probability of false alarm. It is noted that the targets are very sparse in the data set, present only a few percent of the time, so the results are very similar to probability of false alarm. Figures 6 and 7 show the cumulative distribution functions for the sparse data sets. The results show a clear knee in the curve for the selection of an operating point. Figure 8 shows the joint probability distribution of the detectors for the sparse data set. For initial testing, the operating point was selected at the 5% false alarm rate for the two detectors, which correspond to 1006 for HED and 2754 for DCD.

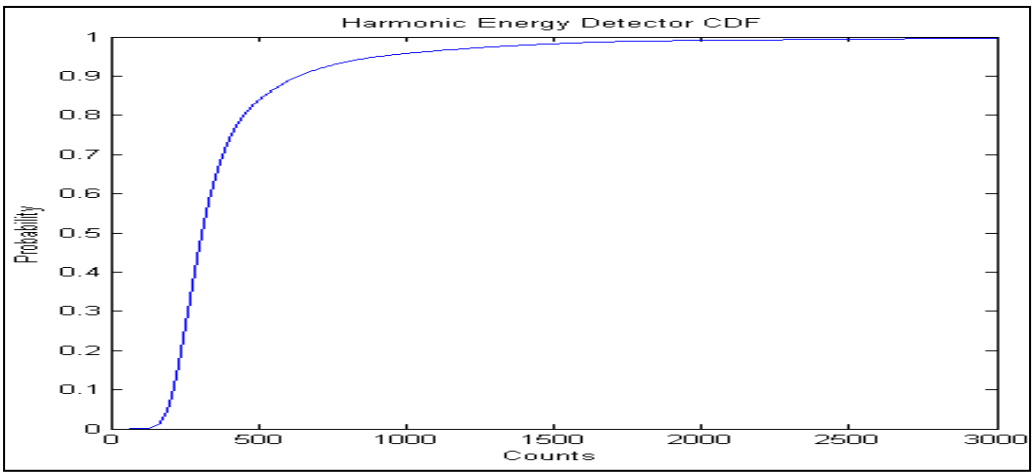

Figure 6. HED cumulative distribution plot, sparse targets.

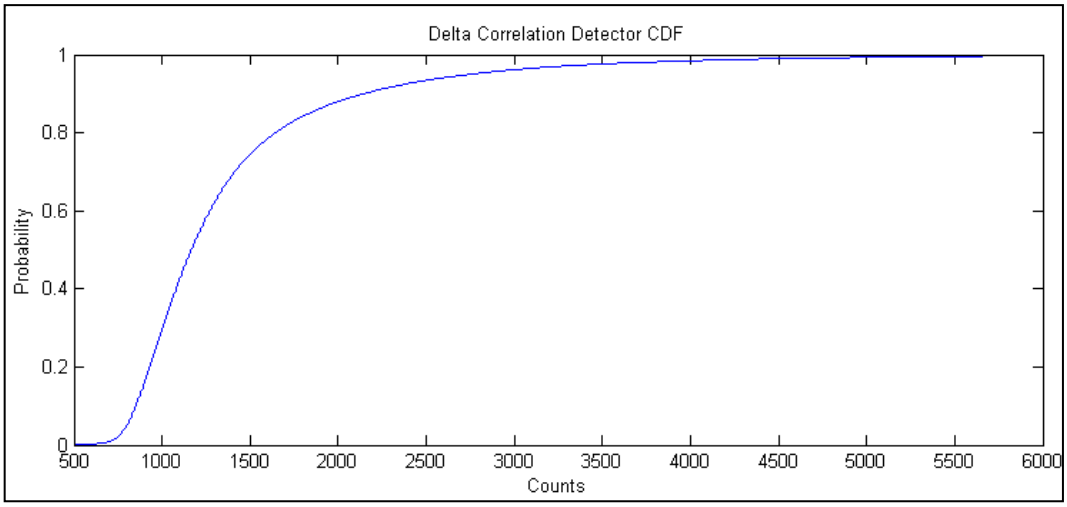

Figure 7. DCD cumulative distribution plot, sparse targets.

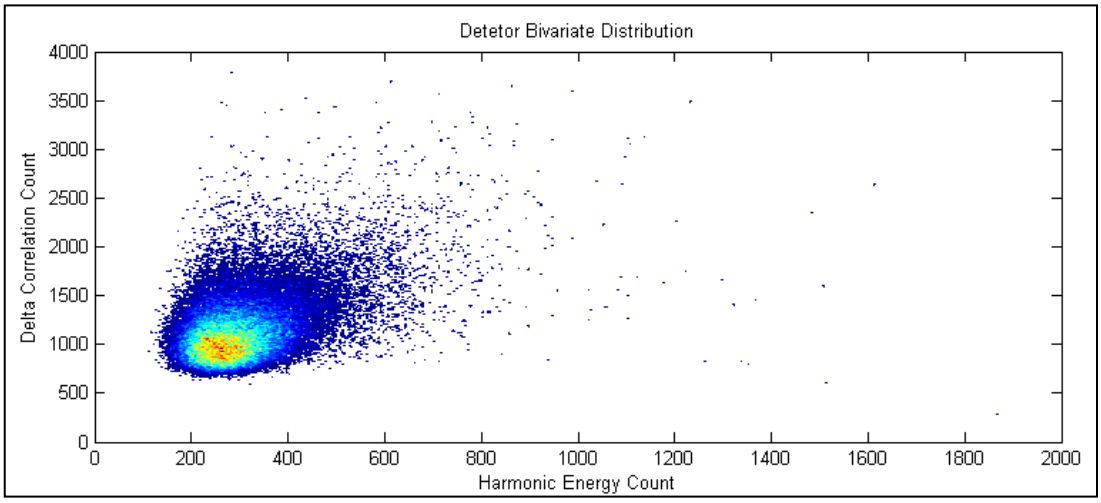

Figure 8. Joint probability distribution plot, sparse targets.

An example of the MATLAB LPAD results is shown in figure 9. The top plot is the spectrogram of the raw acoustic data collected over a 30-min interval. During this time, three primary events occur at approximately 200, 900, and 1400 s. The first event is a water craft leaving the area. The second event is a boat passing by, while the third event is a commercial jet aircraft flying over. The second plot contains the raw output results of both detectors with the HED, shown in blue, and the DCD, shown in red. The bold X's indicates when both detectors are reporting values above threshold levels discussed in the previous section. These joint detections are indicative of when the LPAD would trigger an external device. In the first event, the target is initially stationary, and then accelerates to full speed causing an increase in frequency due to engine RPM. This causes both detectors to fire, as the target moves away from the HED and quickly falls off due to a drop in signal to noise. The DCD continues above threshold for some period as the spectrum isn't constant due to variation in RPM, Doppler, and fading. In the second event,

the target passes by the LPAD at full speed and again both detectors behave in a similar manner, with the joint detection occurring near CPA. The third event doesn't produce a joint detection as the jet engine noise is a broadband structure lacking strong harmonic content. This is considered a positive rejection as distant commercial aircraft can be a significant false alarm even for very remote sensors.

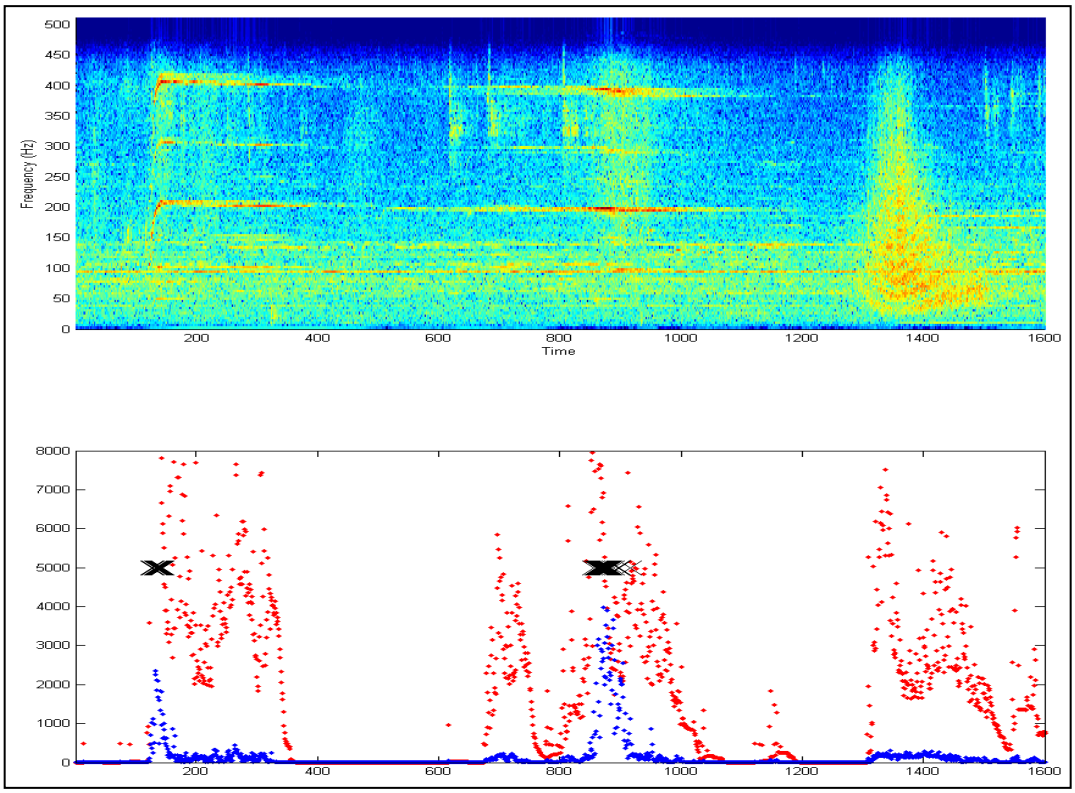

Figure 9. LPAD results for boat and aircraft encounter, X's indicated joint detection criteria meet.

3.2 LPAD Breadboard:

To support engineering development, a LPAD breadboard was developed. The breadboard, shown in figure 10, consisted of three major components: an Actel "Igloo nano Starter Kit" (COTS), a Sparkfun "Logomatic Serial SD DataLogger" (COTS), and an ARL custom LPAD electronics board. The Actel board contained an AGLN250 device and programming tools to support VHDL targeting and debug. The Logomatic recorded UART serial traffic produced by the LPAD, which included detection statistics for both detectors. The LPAD electronics board contains microphone interface, analog filters, comparator, low power oscillator, and power on reset functions.

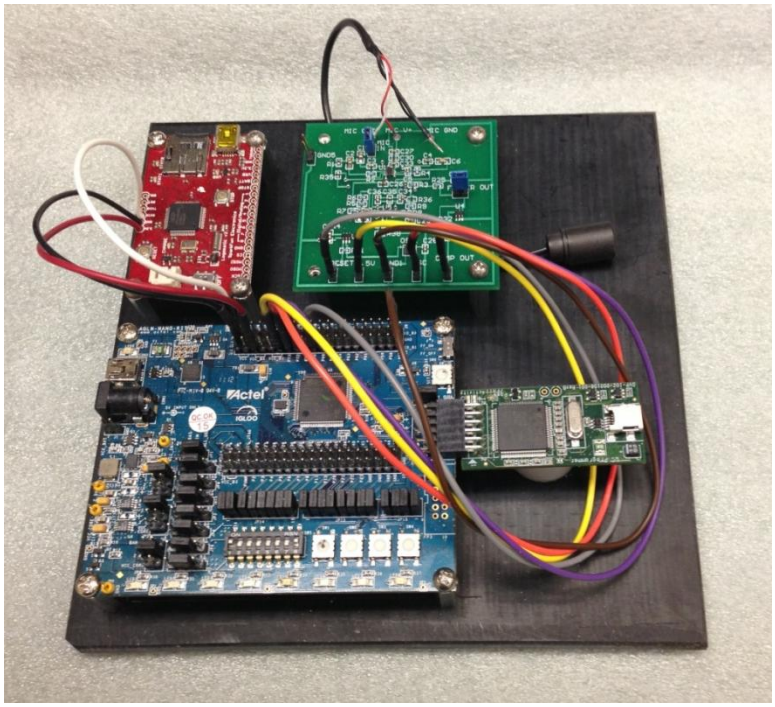

Figure 10. LPAD breadboard.

The LPAD electronics board was used to prototype several analog front end designs and evaluate several candidate op amps. The complete breadboard was used in two primary configurations to support VHDL validation. The first was a “hardware-in-the-loop” setup. External to the breadboard, an arbitrary waveform generator was used to replay recorded analog data directly into the analog front end of the LPAD. Inline attenuators were used to set the receive SPL to produce a repeatable SPL input signal level. The results of the VHDL algorithm were then logged via the Logomatic. This allows repeatable trial runs and direct comparison when the same data file was processed in MATLAB with the reference algorithm. This was the primary means of validating hardware and VHDL performance. The second configuration connected a microphone to the LPAD to process live acoustic data. This allowed quick evaluation against signatures by simply replaying signatures of interest through an audio speaker system.

3.3 Field Verification

To support field evaluations of LPAD, a low-cost data collection system was developed. A commercial “Trail Cam” (TC) was selected as the base of the data collection system due to its ability to record audio and video. The TC is normally triggered by its onboard passive infrared (PIR) sensor. The standard trigger circuit was bypassed and the open collector trigger output from the LPAD was injected into the electronics. This allows the TC to operate as designed but only record data when triggered via the LPAD. The TC was generally configured to collect 30 s of full motion video with audio at every LPAD trigger point. These data are recorded to the TC internal secure digital memory card for post-processing. The recorded files are both time and

date stamped to allow correlation with truth data for known encounters. The raw audio and video tracks allow analysts to determine if a specific trigger event should be scored as a true detect, false alarm, or detection of a non-cooperative target in the test area. The data collection system is shown in figure 11: a modified TC incorporating LPAD. The TC is the black box with the LPAD contained in silver box rear mounted to the unit. Extending from the LPAD box is a microphone arm with windscreen.

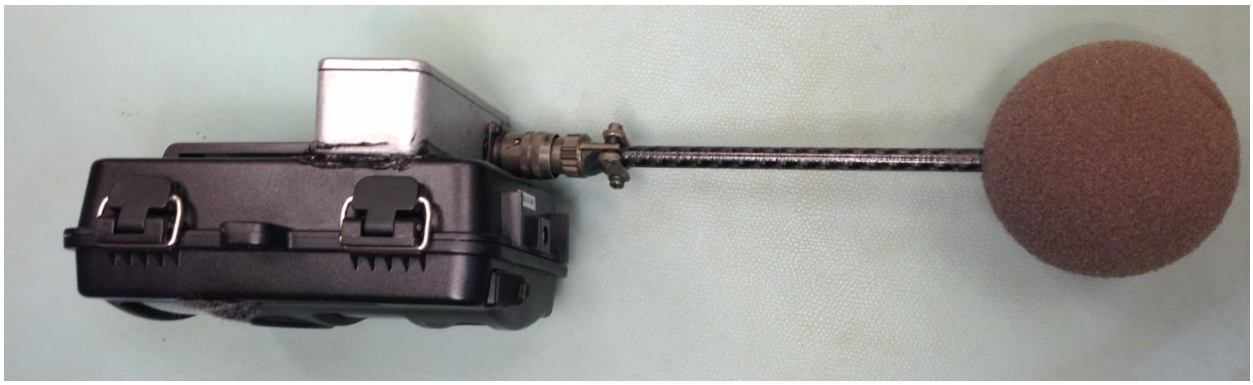

Figure 11. Modified trail camera incorporating LPAD.

3.4 LPAD Measured Power Consumption

The following are the details of the LPAD's power consumption:

- FPGA draws 20 µA at 1.2 V
- Front end draws 65 µA at 2.5 V
- Total power under 190 µW
- Using a lithium AA battery (3 V 2.4 Ah), LPAD will nominally operate for 3 years

4. Conclusions and Future Developments

The LPAD system can significantly extend the operational life of current UGSs as a cost-effective add-on. The FPGA-based design allows the final algorithms to be tailored to specific target and mission requirements. The current embodiment of LPAD provides researches an open architecture platform to evaluate power-efficient acoustic detection algorithms in the field, which extend beyond the HED and DCD presented in this report.

Future developments will include the addition of a low-cost imager. The imager will be used as a second tier of wake-up detection, only being activated upon LPAD event. The low-power imager will allow detection of movement within the field of view prior to alerting additional assets. ARL

plans to test the LPAD against additional target sets in various scenarios such as: runway monitoring, riverine traffic monitoring, ultra-light aircraft detection, and vehicle detection.

5. References

1. Neiswander, P.; Kaiser, S. Acoustic Target Models and Phenomenology. *Proc. SPIE* Vol. 4040, p. 131–141, *Unattended Ground Sensor Technologies and Applications II*, July 2000.
2. Goldberg, D.; Andreou, A.; Julian, P.; Pouliquen, P.; Riddle, L.; Rosasco, R. VLSI Implementation of an Energy-Ware Wake-up Detector for an Acoustic Surveillance Sensor Network. *ASM Transactions on Sensor Networks* **November 2006**, *2* (4), 594–611.

Appendix A. Lower Power Detector Schematics

Figures A-1 through A-4 shows the LPAD schematics.

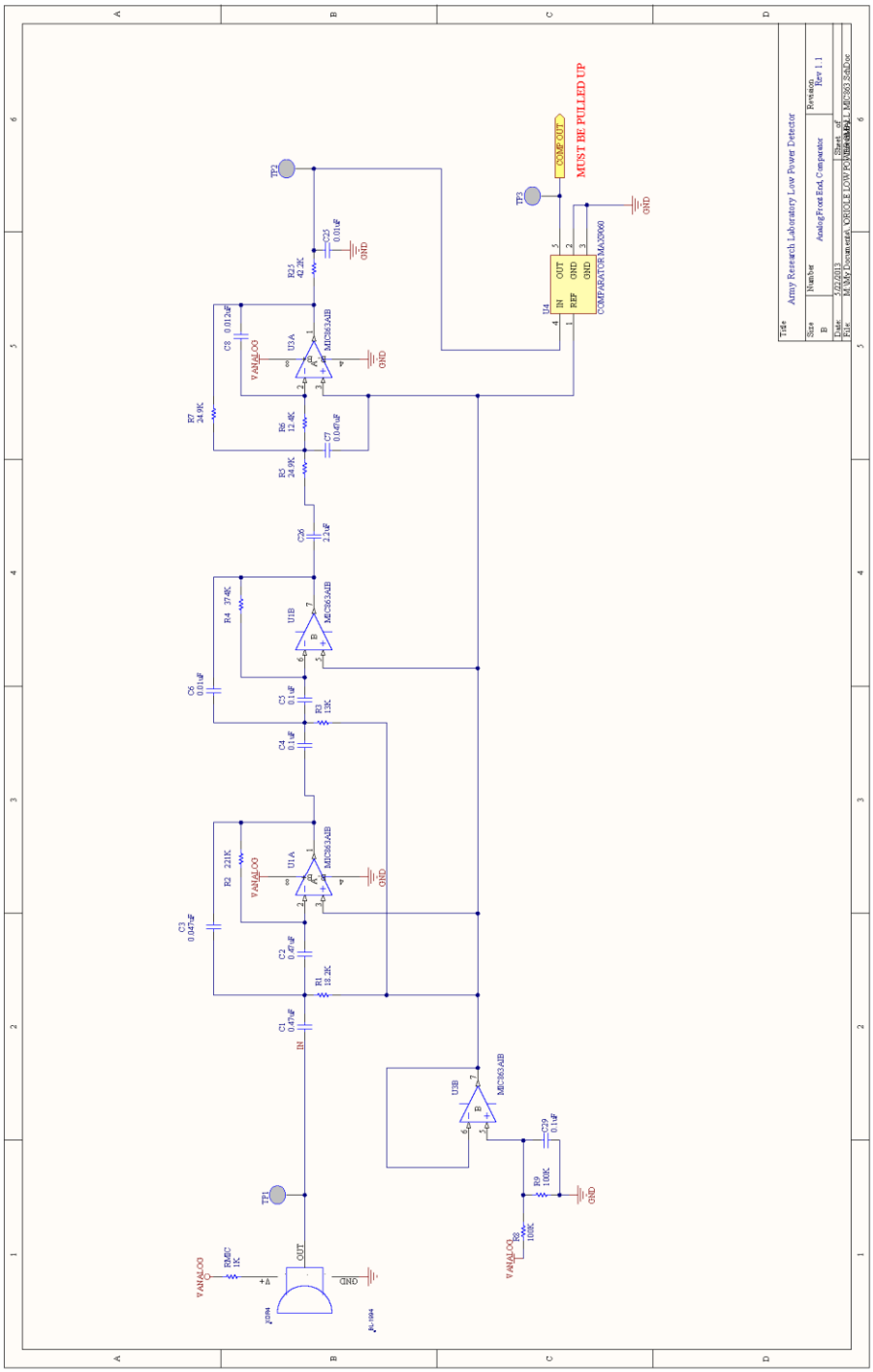

Figure A-1. LPAD schematic sheet 1.

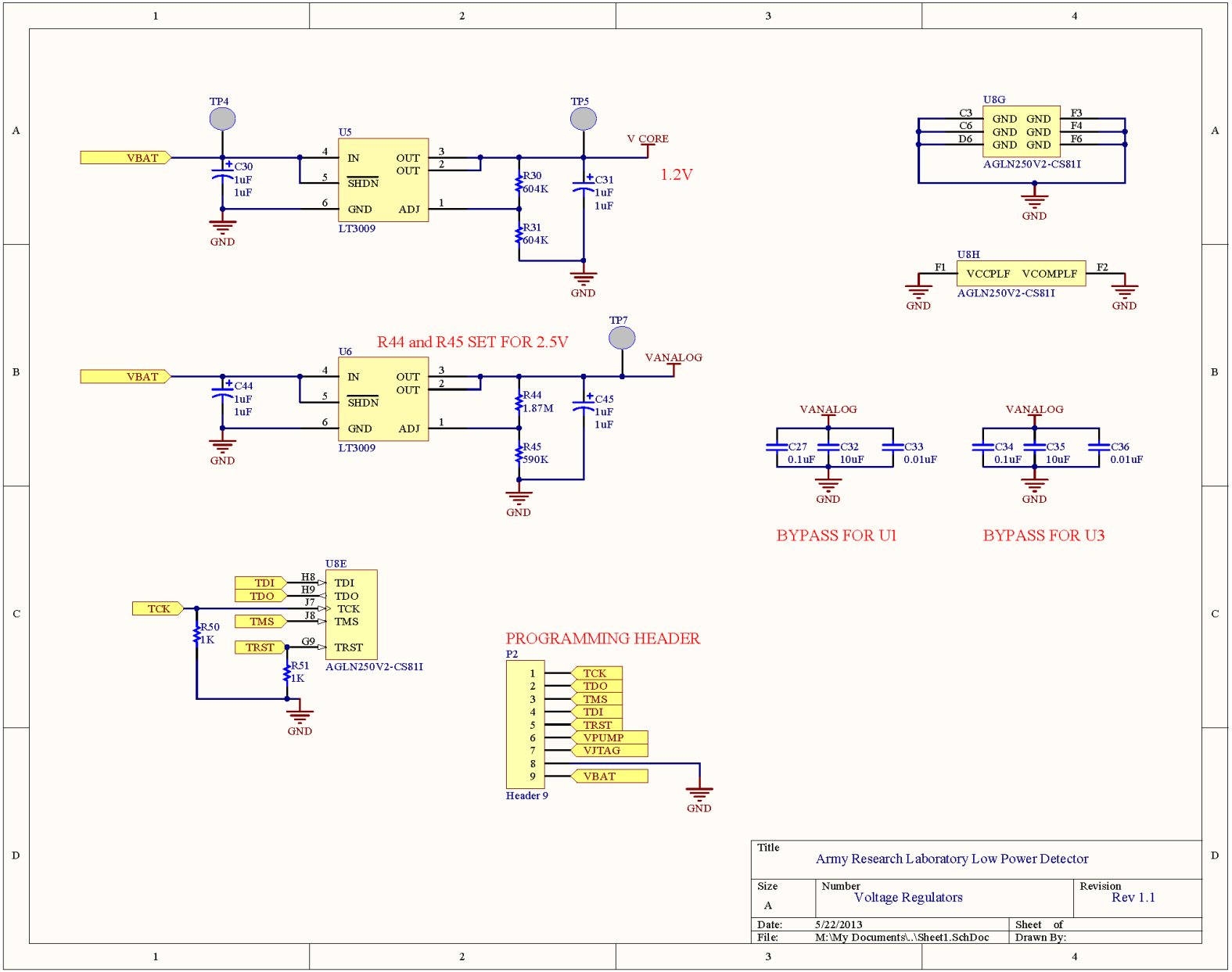

Figure A-2. LPAD schematic sheet 2.

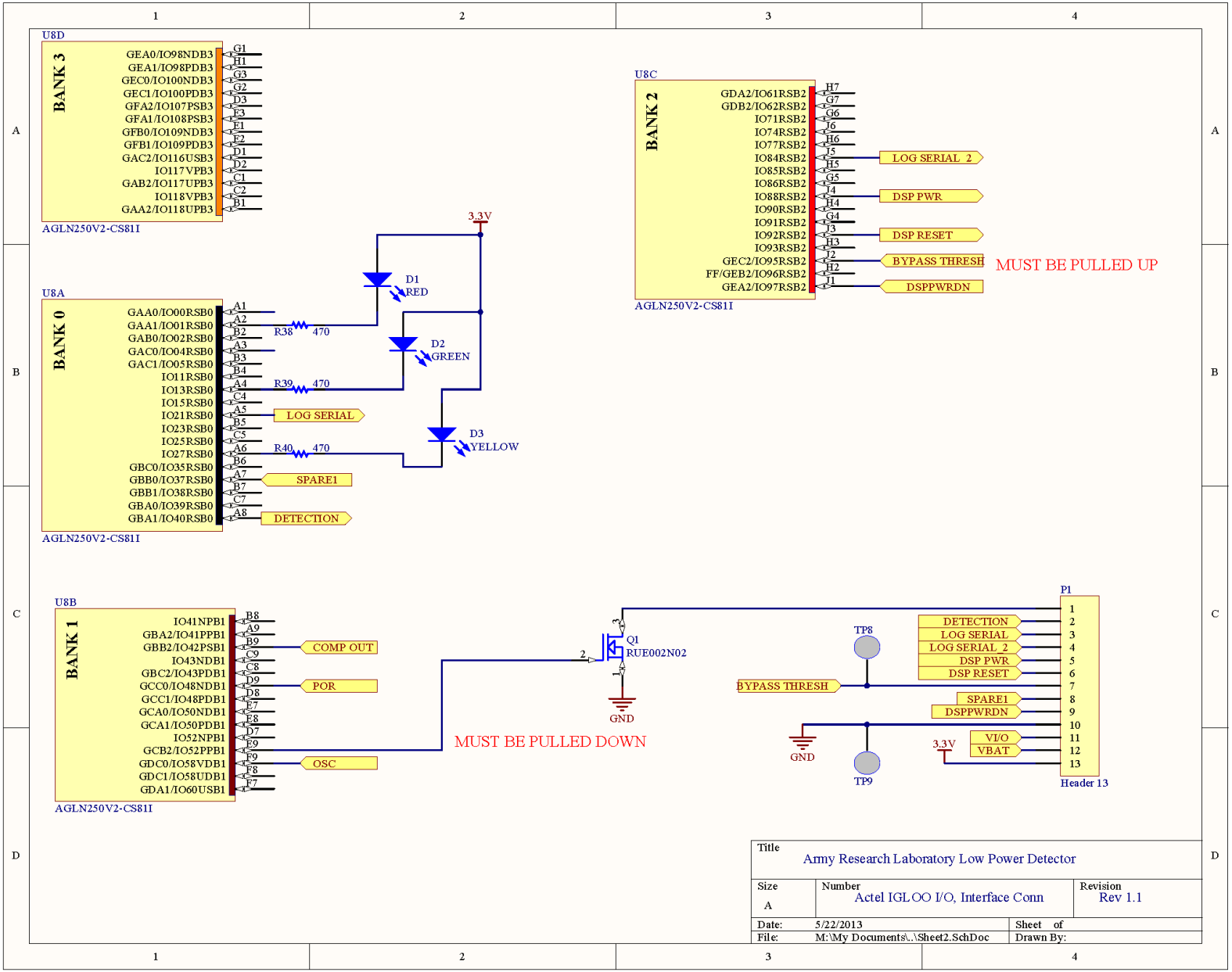

Figure A-3. LPAD schematic sheet 3.

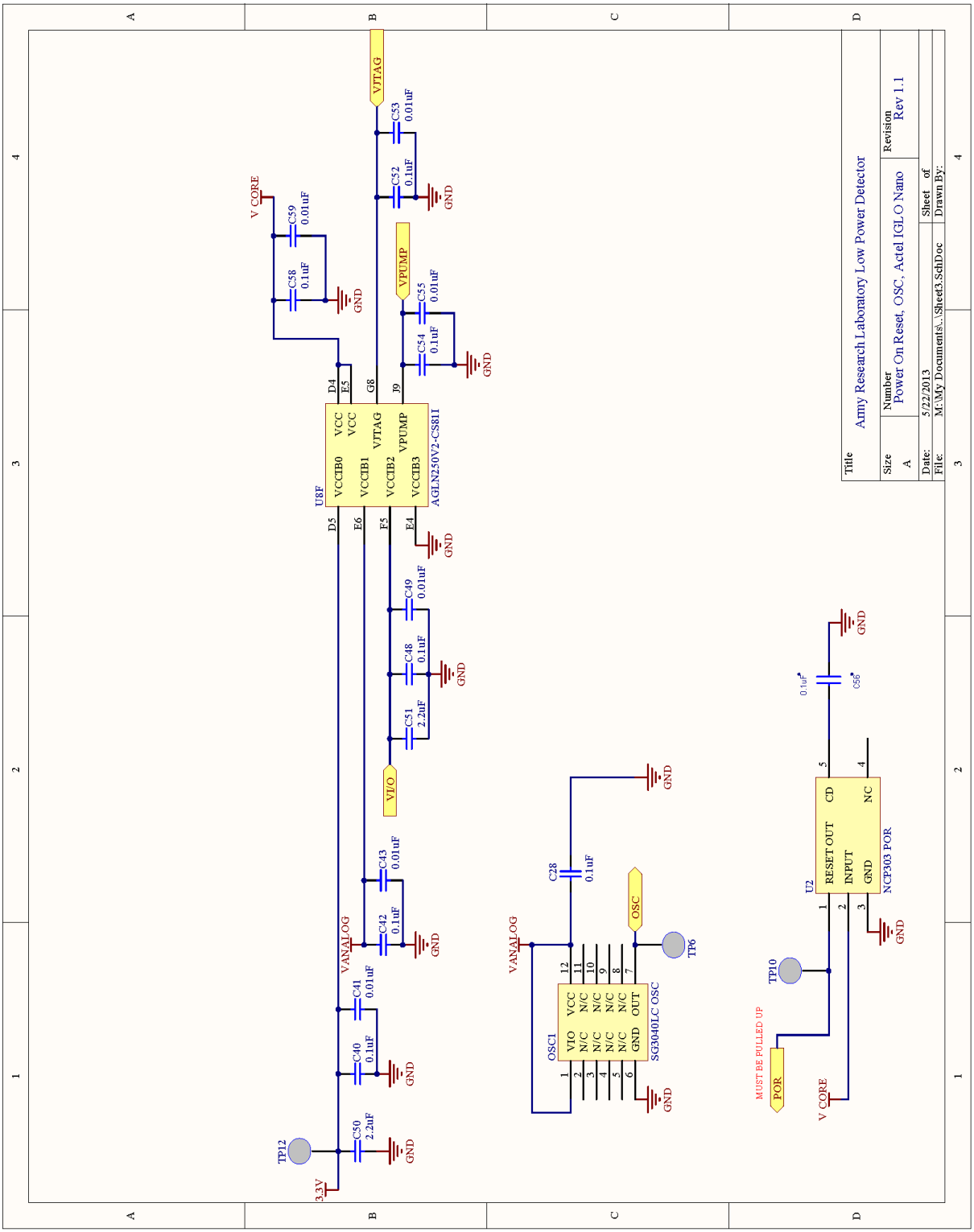

Figure A-4. LPAD schematic sheet 4.

Appendix B. MATLAB Source Code

The following is the MATLAB source code used in the first implantation of the LPAD algorithm.

```
%%%%%%%%%%%%%%%%%%%%%%%%% TestBothDetectors.m %%%%%%%%%%%%%%%%%%%%%%%%%%%%
NumCorrHist = 32;       %max frames in time history for DCD
CorrWin = 30;           %max delay in ACF for DCD
PMThresh =  1006;
DCDThresh = 2754;

%Load in test data and convert to Volts at Mic
%In this case Reftek data with pre-amp of G=50;
data=load('E14S0C1.dat');
data = data*20/2^24;
data = data'/50.0;
DetCh = 1;

%Remove DC offset in data; Comparator assumes threshold at 0 Volts
data(DetCh,:) = data(DetCh,:) - mean(data(DetCh,:));

numblocks = floor(max(size(data(1,:)))/1024)-5;
%Initialize Results Buffers
TargetLP=zeros(numblocks,1);
Palt=zeros(numblocks,1);
Palt1Bit=zeros(numblocks,1);
DCD1Bit=zeros(numblocks,1);
CorrDiff=zeros(numblocks,NumCorrHist);
CorrBuff=zeros(NumCorrHist,CorrWin);

%process through 1 second blocks of data
for i=1:numblocks
    data1Sec = (data(:,i*1024:(i+1)*1024 - 1));

    %Run PM detector
    [Palt(i) Palt1Bit(i) Xcorr1Bit] = LowPowerDetectorBTM(...
                                                data1Sec(DetCh,:), 1024);
    %Retain 1Bit Rxx values for DCD detector
    if i == 1 %to avoid startup transients prefill buffer with first value
        CorrBuff = repmat(Xcorr1Bit(1:CorrWin)',NumCorrHist,1);
    else
        CorrBuff = [Xcorr1Bit(1:CorrWin)'; CorrBuff(1:(end-1),:)];
    end

    %Run DCD detector
    for lag=1:NumCorrHist
        CorrDiff(i,lag) = (mean(abs(CorrBuff(1,:) - CorrBuff(lag,:))));
    end
    DCD1Bit(i) = sum(CorrDiff(i,:));
```

```
    %Evaluate against selected detector thresholds
    if (Palt1Bit(i) > PMThresh ) && (DCD1Bit(i) > DCDThresh )
        TargetLP(i) = 1; %Mark Joint Detection
    end
end
%Plot Results:
%1)Spectrogram for reference
%2)Results from both PM and DCD and locations of joint detections
figure
subplot(2,1,1)
spectrogram(data(DetCh,:),1024,0,256,1024,'yaxis')
axis('tight')
subplot(2,1,2)
%Plot DCD detector results
plot(sum(CorrDiff,2),'r.')
hold
%Plot PM detector results
plot((Palt1Bit),'b.')
%Find location of joint detections an plot
tagi=find(TargetLP>.5);
plot(tagi,5000*ones(1,length(tagi)),'kx','MarkerSize',20)
axis tight
%%%%%%%%%%%%%%%%%%%%%%% End of TestBothDetectors.m %%%%%%%%%%%%%%%%%%%%%%%%%

function [ Palt Palt1Bit Rx1Bit] = LowPowerDetectorBTM( data,sampRate)
    MinFreq = 50;    % range for peak detector
    MaxFreq = 300;
    NMin = floor(sampRate/MaxFreq);
    NMax = ceil(sampRate/MinFreq);
    %Compute ideal Power Measure
    Rx = xcorr(data,'coeff');
    Rx = Rx(sampRate:end);
    ideal = (diff(Rx).^2);
    Palt = sum(ideal(NMin:NMax));
    %Compute 1 bit Power Measure
    HystThres = 0.012;
    [ data1Bit ] = Comparator(data,HystThres);
    Rx1Bit=zeros(sampRate,1);
    for i=1:sampRate
       K = sampRate  - i;
       Rx1Bit(i) = sum(not(xor(data1Bit(1:K),data1Bit(i+1:end))));
    end
    Nonideal = (abs(diff(Rx1Bit)));
    Palt1Bit = sum(Nonideal(NMin:NMax));
end

function [ OneBitData ] = Comparator(data,HystThres)
    %Convert to volts at converter, low power detector G=100;
    data = data*100;
    OneBitData=zeros(1,length(data));
    OneBitData(1) = OneBitData(1) > 0;
    for n = 2:length(data)
        if data(n) > HystThres
            OneBitData(n) = 1;
        elseif data(n) < -HystThres
            OneBitData(n) = 0;
        else
```

```
            OneBitData(n) = OneBitData(n-1);
        end
    end
end
```

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Appendix C. FPGA Top-Level Schematic

Figure C-1 shows the complete top-level schematic of the FPGA implementation.

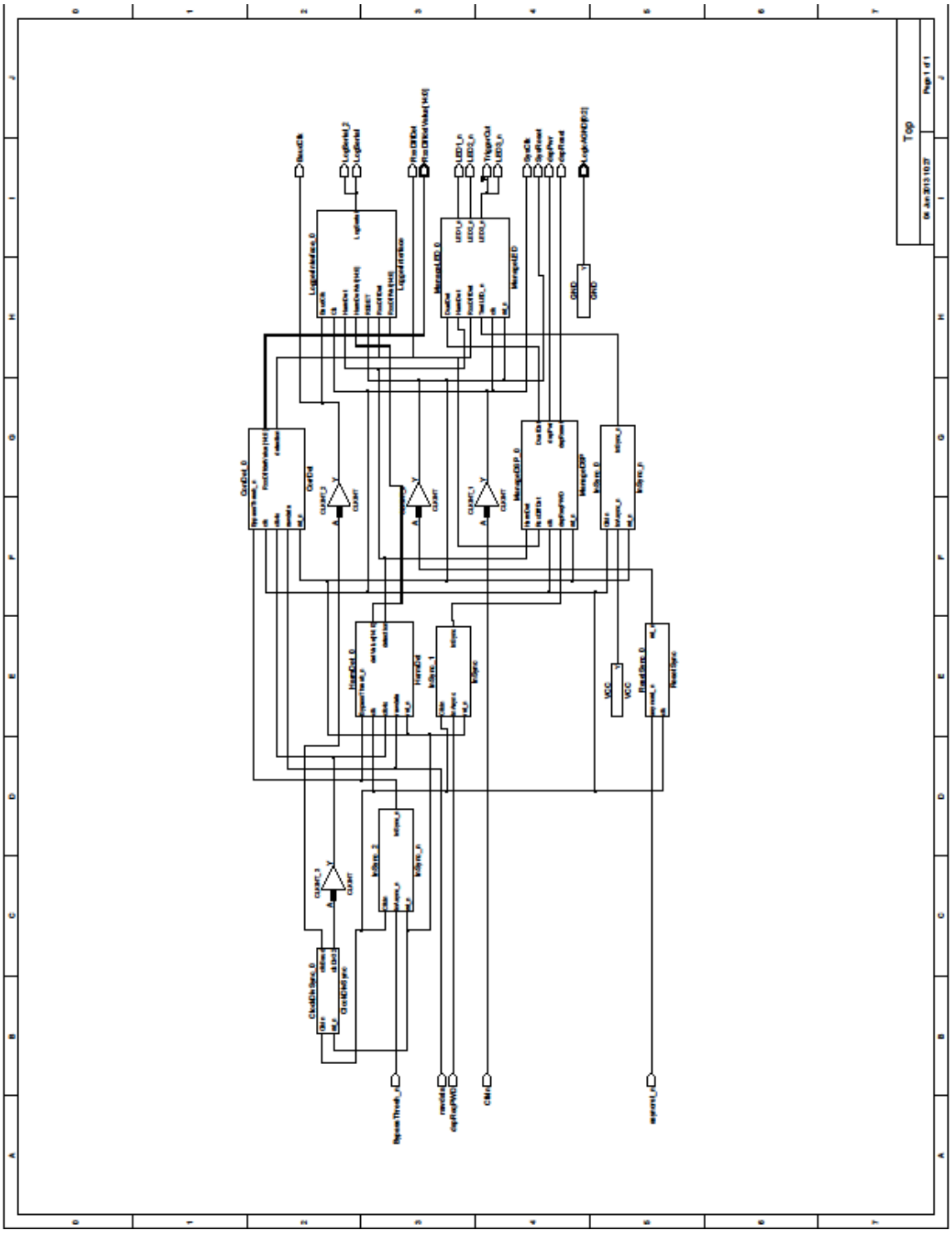

Figure C-1. FPGA top-level schematic.

List of Symbols, Abbreviations, and Acronyms

A/D	analog to digital
ACF	autocorrelation function
ARL	U.S. Army Research Laboratory
COTS	commercial-off-the-shelf
CPA	closest point of approach
DCD	delta correlation detector
FPGA	field-programmable gate array
GBW	gain bandwidth product
GOTS	Government-off-the-shelf
HED	harmonic energy detector
ISR	intelligence, surveillance, and reconnaissance
LPAD	low-power acoustic detector
PIR	passive infrared
PM	periodic measure
SPICE	Simulation Program with Integrated Circuit Emphasis
SPL	sound pressure level
TC	Trail Camera
UART	universal asynchronous receiver transmitter
UGS	unattended ground sensors
VHDL	VHSIC Hardware Description Language
VHSIC	very high speed integrated circuit

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